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Performance Characterization of Schottky Tunneling Graphene Field Effect Transistor at 60 nm Gate Length

(Pencirian Prestasi Saluran Schottky Grafin Transistor pada Panjang Get 60 nm)

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ABSTRACT

A planar Graphene Field-Effect Transistor GFET performance with 60 nm gate length was evaluated in discovering new material to meet the relentless demand for higher performance-power saving features. The ATHENA and ATLAS modules of SILVACO TCAD simulation tool was employed to virtually design and assess the electrical performance of GFET. The developed model was benchmarked with the established results obtained from the DESSIS simulator model by using the same graphene channel's parameters and simulated at fixed threshold voltage of 0.4V. The GFET was also analyzed and ranked its performance for four different gate oxides which includes HfO_2, Al_2O_3, TiO_2, and Ta_2O_5. Compared to the benchmarked device, our GFET shows a competitive performance although it possesses a lower drive current (I_{ON}). However, the leakage current (I_{OFF}), subthreshold swing (SS) and the device's switching capability (I_{ON}/I_{OFF}) are more superior than those of the benchmarked device, with an improvement of 99%, 48.3% and 99.36%, respectively. The with different gate dielectrics were also proven to possess a lower I_{OFF}, competitive I_{ON}, smaller SS and better switching capability compared to the established DESSISS model. The graphene parameters in this experiment can be utilized for further optimization of GFET with smaller gate lengths.

Keywords: Graphene; high-k dielectric; SILVACO

ABSTRAK

Prestasi satah panjang pintu 60 nm Grafin transistor GFET dinilai dalam pelapisan bahan baru untuk memenuhi permintaan yang tidak henti-henti untuk ciri-ciri penjimatan prestasi kuasa yang lebih tinggi. GFET yang dianalisis menggunakan ATHENA dan ATLAS modul dalam perisisan Silvaco TCAD mereka bentuk transistor dan menilai prestasi elektrik. Model yang dibangunkan ditanda aras dengan keputusan mantap daripada perisian DESSIS model dengan menggunakan parameter saluran grafin yang sama dan simulasi pada voltan ambang tetap 0.4V. Prestasi GFET juga dianalisis di empat oksida pintu yang berbeza yang termasuklah HfO2, Al2O3, TiO2 dan Ta2O5. Keputusan peranti menunjukkan prestasi peranti yang berdaya saing dengan peranti asas dan parameter struktur walaupun ia mempunyai arus semasa yang lebih rendah (I_{ON}). Kebocoran arus (I_{OFF}), sub ambang swing (SS) dan keupayaan pensuisan peranti (I_{ON}/I_{OFF}) bagaimanapun telah menunjukkan ciri peranti besar dengan peningkatan masing-masing sebanyak 99%, 48.3% dan 99.36%. Keputusan menggunakan dielektrik pintu yang berbeza juga menghasilkan I_{OFF} yang lebih rendah, I_{ON} yang berdaya saing,, SS yang lebih kecil dan keupayaan pensuisan yang lebih baik berbanding model DESSISS yang ditubuhkan yang mana parameter grafin dalam eksperimen ini boleh digunakan untuk pengoptimuman dan mereka bentuk peranti dengan panjang pintu yang lebih kecil.

Kata kunci: Dielektrik tinggi-k; grafin; SILVACO

INTRODUCTION

The geometrically downscale of planar devices through Moore's Law have led to an innovation of new architectures and materials. The adoption of high-k metal gates materials and three-dimensional (3D) devices such as tri-gate have been successful approaches for boosting the transistor performance. Nevertheless, their issues on leakage current and doping levels may not provide significant improvement in the performance of transistors below the 22 nm node. The high mobility of Carbon Nanotube (CNT) material was then proposed as an alternative material (Durkop et al. 2004). In spite of its advantage, accurate placement of CNT and its conductivity which depends on its chirality making them a doubtful candidate for Ultra Large Scale Integration (ULSI) trade. Graphene material has recently gained a lot of attention due to their potential as switching devices for impending planar technology nodes. It was introduced as a channel material in a transistor to counter the problems and have been reported (Cheli et al. 2009; Ferrari et al. 2006; Fiori et al. 2014; Noor Faizah et al. 2016a; Zhu & Woo et al. 2007). Graphene was found to be the most reliable material thus far with single layer of Carbon behavior, resulting in outstanding gate control over the channel (Cheli et al. 2009; Ferrari et al. 2006; Fiori et al. 2014). However, the device may suffer a very low switching capability of on-state current (I_{ON}) to leakage

current (I_{OFF}) ratio due to the absence of an energy gap (Fiori et al. 2014; Nemes-Incze et al. 2008). Top-gated layers and a high concentration of Si was then introduced to overcome the problem. The function of the top gate was to modulate the drain current and limit the carrier mobility. The employment of high concentration of Si on the other hand was to accumulate the S/D Schottky tunnelling for low resistive path such that only electrons or holes will be inoculated into the graphene channel and thus yield a unipolar conduction (Zhu & Woo 2007). Therefore, a reasonable I_{OFF} can be attained while maintaining a high I_{ON}. In this work, the performance of 60 nm graphene transistors was benchmarked with the established DESSIS model (Zhu & Woo 2007) to create a platform for future device analysis at different gate length by using the same graphene properties established in this simulation. The final results were assessed and compared in terms of its drive current (I_{ON}), leakage current (I_{OFF}), subthreshold swing (SS) and switching capability (I_{ON}/I_{OFF}). To allow comparison of the two model and to strengthen the conclusion, our device was simulated at fixed threshold voltage of 0.4V, following the benchmarked device. In order to get the V_{TH} to 0.4V, doping concentration of three processing parameters was first varied. Recent work done by Afifah Maheran et al. (2014) and Noor Faizah et al. (2016a) through Taguchi optimization method also proved that these parameters hold the key performance of the transistor and was viable to adjust the V_{TH} value closer to the prediction. These parameters are Halo implantation dose, S/D implantation dose and compensation implantation dose. Further assessment was then made to investigate the best dielectric material which gave the finest performance when harmonizing with graphene layers. The dielectric materials that were employed and studied in this experiment includes hafnium dioxide (HfO_2; k~22), aluminum oxide (Al_2O_3; k~9.3), titanium dioxide (TiO_2; k~80) and tantalum pentoxide (Ta_2O_5; k~26). Here, the V_{TH} was maintained at 0.4V by process parameters variation. Graphene layer characterization was partially calculated and assumed to displays an ideal ohmic contact and functioned at a ballistic transport. The virtual device was constructed using ATHENA module and characterized by ATLAS module of SILVACO TCAD tools. Final results were confirmed through the benchmarking with the established DESSIS model of the same gate length, displaying a better performance and could be enhanced for better transistor characterization.

METHODS

In this study, the fabrication of graphene n-type MOSFET through ATHENA module follows the same conventional top-down transistor compatible process flow (Afifah Maheran et al. 2014; Noor Faizah et al. 2016b). Initially, a <100> orientation substrate of boron-doped silicon was created. Then the substrate was thermally oxidized to form a silicon dioxide (SiO_2) layers besides to diminish the short channel effect (SCE) which was triggered by the expansion of the depletion layer within the substrate. Next, a pristine layer of graphene was placed on top of the SiO_2 layer. Figure 1 shows the doping profile of HfO_2/WSi_2 graphene field effect transistor at 60 nm gate length. Note that the physical characterization of graphene layers utilized in this experiment followed the benchmarked DESSIS model where a single layer of graphene is set at 3.37Å thickness with zero bandgap, modeled as a semi-metal material. The saturation velocity was set at 10 ^{8}cm/s, a fairly large value of 100 ns for radiative recombination lifetimes of the electron and hole and a 15000 cm^2/Vs for its carrier mobility. The electron and hole densities of states of graphene were measured at a temperature of 300K (Zhu & Woo 2007).

$$Nc = \frac{8\pi m_e kT}{h^2}\ln(1+e^{-(Ec-Ef)/kT}) \qquad Nv = \frac{8\pi m_h kT}{h^2}\ln(1+e^{-(Ef-Ev)/kT}) \quad (1)$$

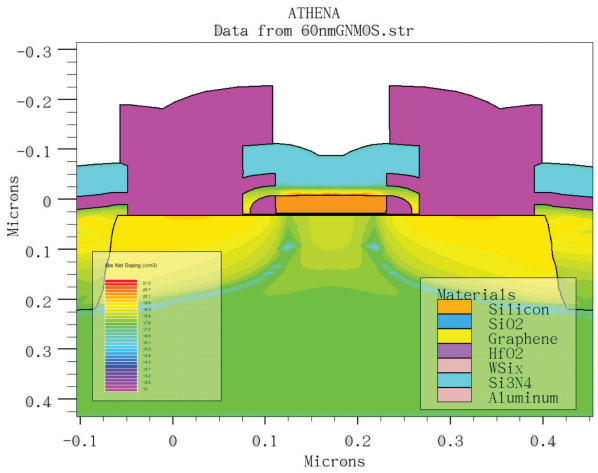

FIGURE 1. Doping profile of graphene field effect transistor

The effective masses of electrons and holes in graphene in this study were set at $m_e \approx 0.05\ m_o$, $m_h \approx 0.04 m_o$ and m_o is the free electron mass. Experimentally, the number of electrons and holes per unit area was found to be ~10^{12}/cm^2, which agrees with that reported in (1) (Berger et al. 2004). The graphene layer was assumed to exhibit a perfect ohmic contact and function at a ballistic transport. Four different High-k dielectric materials of 2 nm thicknesses, which includes hafnium dioxide (HfO_2), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2) and tantalum entoxide (Ta_2O_5), was then sandwiched between the graphene layer and the 77.1 nm thick Tungsten Silicide (WSi_2) metal gate in separate experiments to fabricate four n-type MOSFET devices. After WSi_2 deposition, both High-k metal gate materials layers were etched precisely to produce a 60 nm (±0.1 nm)-length transistor. Next, Halo implantation was doped with Indium material to reduce the short channel effect (SCE). Arsenic was then

implanted at high concentration to accumulate the Schottky tunneling of the source-drain (S/D) regions. The purpose was to create a tunneling effect which offered a smoother path for only either electrons or holes to be injected into the tunnel and thus achieved a unipolar conduction. The final process took place right after the growth of 0.05 um-thickness of boron-phosphor-silicate-glass (BPSG) and a compensation implantation which was doped with Phosphorus material. At this stage, the metal contacts were formed and etched accordingly using aluminum layer. The device was then ready for its electrical characterization through ATLAS module. The first analysis was to measure the V_{TH} value as it was the main criteria for assessment and comparison with the benchmarked device. To retain the threshold voltage (V_{TH}) within the targeted value of 0.4V, the doping concentrations of Halo implantation, S/D implantation and Compensation implantation were varied accordingly. Each of the doping values depends on the High-k material as they possess a different properties and k-value. A comprehensive fabrication procedure of the design was summarized in Table 1. The design of factor variations on the other hand was summarized in Table 2. For a clearer view, its dopant level which was varied to retain the V_{TH} value was illustrated in Figure 2. It can be observed that Al_2O_3 utilized the highest S/D implantation dose compared to other materials.

Results and Discussion

This section shows the electrical characterizations of the 60 nm n-type graphene MOSFET attained from the ATLAS module of SILVACO TCAD Tools. The results were compared with the established DESSIS simulator MOSFET model using the same graphene's parameters to set a platform for future

TABLE 1. GFET fabrication procedure

Process Step	n-type MOSFET parameters
Substrate	• Silicon • <100> orientation
Retrograde well implantation	• 200 Å oxide screen by 970°C, 20 min of dry oxygen • 4.5×10^{11} cm^{-3} phosphorous • 30 min, 900°C diffused in nitrogen • 36 min, dry oxygen
STI isolation	• 130 Å stress buffer by 900°C, 25 min of dry oxygen • 1500 Å Si_3N_4, applying LPCVD • 1.0 um photoresist deposition • 15 min annealing at 900°C
Gate oxide	• diffused dry oxygen for 0.1 min, 815°C
Vt adjust implant	• 1.75×10^{11} cm^{-3} Boron difluoride • 5 KeV implant energy, 7° tilt • 20 min annealing at 800°C
Graphene layer	• 0.000377 um graphene
High-K/Metal gate deposition	• 0.002 um high-K dielectric • 0.038 um WSi_2 • 17 min, 900°C annealing
Halo implantation	• 4.876×10^{13} cm^{-3} indium • 19.79° tilt
Sidewall spacer deposition	• 0.047 um Si_3N_4
S/D implantation	• 1.41×10^{13} cm^{-3} arsenic • 10 KeV implant energy • 7° tilt
PMD deposition	• 0.05 um BPSG • 20 min, 850°C annealing • 1.1×10^{12} cm^{-3} phospor • 60 KeV implant energy • 7° tilt
Metal 1	• 0.04 um aluminum
IMD deposition	• 0.05 um BPSG • 15 min, 950°C annealing
Metal 2	• 0.12 um aluminum

TABLE 2. Factors variation of different dielectric material

k	Dielectric material	Doping concentration (atom/cm^3)		
		Halo implantation	S/D implantation	Compensation implantation
22	HfO_2	8.56×10^{13}	1.74×10^{14}	0.65×10^{14}
9.3	Al_2O_3	7.5×10^{13}	2.0×10^{14}	0.705×10^{14}
80	TiO_2	9.72×10^{13}	1.7×10^{14}	0.64×10^{14}
26	Ta_2O_5	8.75×10^{13}	1.7×10^{14}	0.65×10^{14}

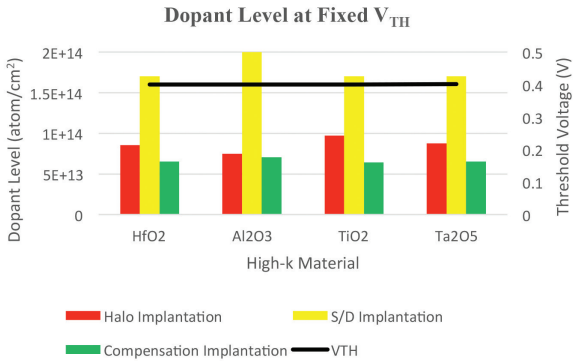

FIGURE 2. Factors variation of different dielectric material at fixed V_{TH}

graphene's transistor. In order to strengthen the findings and the conclusions besides allowing the comparison of the device performance, the applied threshold voltage (V_{TH}) in this research was also set at the same value as that of the benchmarked device, which was fixed at 0.4V. The only device variation was on the utilization of the dielectric materials. The effect of different dielectric materials onto the graphene layers and the dependencies on process parameters were also studied and analyzed in this part. Figure 3 shows the curve of the drain current (I_D) against the gate voltage (V_{GT}) and Figure 4 shows the curve of subthreshold I_D-$V_{GT.}$ Both distinctive graphs were simulated at different V_D of 0.5V and 1.0V. The results of drive current (I_{ON}) and leakage current (I_{OFF}) were extracted from the characteristic curves of Figure 4. I_{ON} was measured at V_D= 1.0V and I_{OFF} is measured at V_D= 0.5V. From the graph, it was observed that the value of I_{ON} was at 0.257249×10^{-3}A/um and the value of I_{OFF} was at 0.23525×10^{-7}A/um. The subthreshold swing (SS) was also extracted from the subthreshold I_D-V_{GT} curve where it was computed through (2) (Kaharudin et al. 2016).

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})}\right]. \tag{2}$$

This parameter was one of significant quality in MOSFET technology as it indicates the switching speed of a device. The theoretical limit of SS in MOSFET is 60 mV/dec

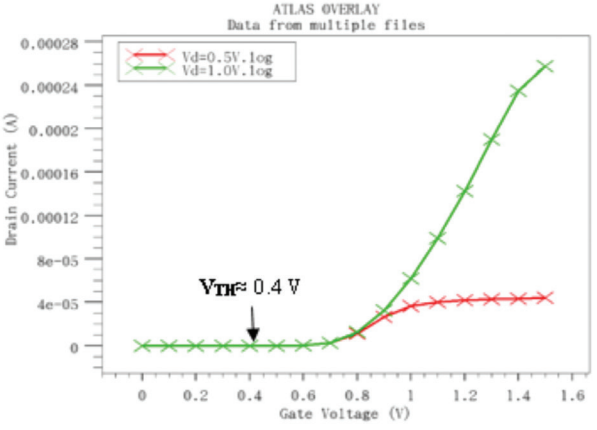

FIGURE 3. I_D-V_{GT} of GFET at different V_D

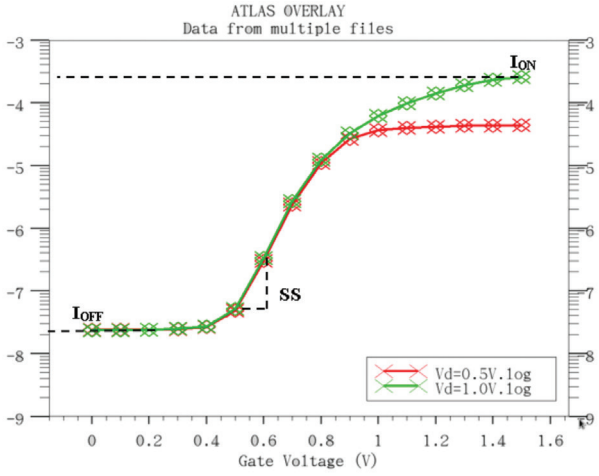

FIGURE 4. I_D-V_{GT} of GFET at different V_D with I_D in log scale

at room temperature. However, a smaller SS is desirable. The value of SS that was extracted from the curves was 110.035 mV/dec. Figure 5 illustrates the characteristic curve of the drain current (I_D) against the drain voltage (V_D) of the fabricated device at different gate voltage (V_{GT}). The applied V_{GT} in this study were 0.2 V, 0.4 V, 0.6 V, 0.8 V and 1.0 V. As seen in Figure 5, at V_{GT}= 0.6 V, the device goes into saturation region when V_D is greater than 0.2 V which is comparable to the benchmarked DESSIS model. This is due to the high electron mobility in the channel despite of the large electron saturation velocities (Zhu & Woo 2007). The first investigation of the simulation of SILVACO TCAD Tools model utilized hafnium dioxide (HfO_2) as the High-k material. The results of the simulated device for performance comparison in terms of I_{ON}, I_{OFF}, SS and I_{ON}/I_{OFF} ratio which utilizing the same graphene's parameters as the DESSIS model are tabulated in Table 3 while the results of the transistor utilizing different High-k materials can be seen in Table 4.

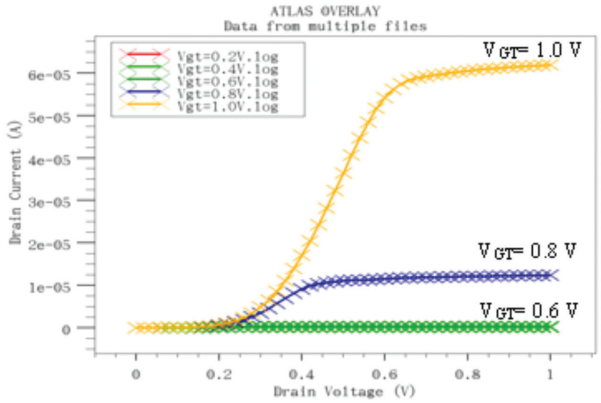

FIGURE 5. I_D-V_D of GFET at different V_{GT}

As can be seen in Tables 3 and 4, the simulation results which were extracted from ATLAS show that the device possesses a lower leakage current (I_{OFF}) of 23.525n, 0.56606p, 23.505n and 23.522n A/um for HfO_2, Al_2O_3, TiO_2 and Ta_2O_5, respectively, as compared to 0.05mA/um of the benchmarked DESSIS model. The results for subthreshold swing of 110.035, 89.54, 104.74 and 109.23 mV/dec for HfO_2, Al_2O_3, TiO_2 and Ta_2O_5, respectively, also scores far lower than 220 mV/dec of the benchmarked device due to the utilization of High-k material to limits the current modulation in the channel. In fact, Al_2O_3 shows a nearer value to the theoretical limits of 60 mV/dec. However, for drive current (I_{ON}), only HfO_2 and TiO_2 with a value of 257.43m and 206.81m A/um, respectively, notches a higher value than 8.5m A/um of DESSIS model. Al_2O_3 and Ta_2O_5 on the other hand has a lower I_{ON} with a value of 0.33467m and 0.24952m A/um, respectively. Further calculation was made to measure the switching capability of the device by defining the I_{ON} to I_{OFF} ratio of the device and therefore concludes the best High-k material to be applied in order to have a high enough drive current with reasonable leakage. In line with the International Technology Roadmap for Semiconductor (ITRS), the device is suitable for high performance logic circuit if the I_{ON} to I_{OFF} ratio is higher than 10^4. This means that the higher ratio value indicates the better device performance. The results showed that of all the four materials, Al_2O_3 scores the highest I_{ON} to I_{OFF} ratio (10^8), followed by HfO_2 (10^7), TiO_2 (10^6) and Ta_2O_5 (10^4). This means, all the High-k candidates show an excellent device performance with Al_2O_3 as the best material to be utilized as the top gate for the highest switching capability with reasonably high I_{ON}, lowest I_{OFF} and competitive SS as compared to the DESSIS model. For a clearer view, the results are illustrated in Figures 6 and 7, respectively. Figure 6 shows the I_{ON}, I_{OFF} and SS results while Figure 7 shows the I_{ON} to I_{OFF} ratio at

TABLE 3. Results of the n-type MOSFET with HfO_2 High-k material

Performance parameter	Device simulator		% of Improvement
	DESSIS Model	Silvaco TCAD Tools Model	
I_{ON}	8.5 mA/um	0.257429 mA/um	96.9
I_{OFF}	0.05 mA/um	23.525 nA/um	99.95
SS	≈ 220 mV/dec	110.035 mV/dec	49.98
I_{ON}/I_{OFF}	0.17×10^3	10.9×10^3	98.44

TABLE 4. Device performance with different dielectric material

Materials	V_{TH}	Performance parameter			
		I_{ON} (mA/um)	I_{OFF} (nA/um)	SS (mV/dec)	I_{ON}/I_{OFF}
HfO_2	≈ 0.4 V	257.429	23.525	110.035	1.09×10^7
Al_2O_3		0.334672	0.00056606	89.5396	5.91×10^8
TiO_2		206.814	23.505	104.738	8.8×10^6
Ta_2O_5		0.249517	23.522	109.233	1.06×10^4

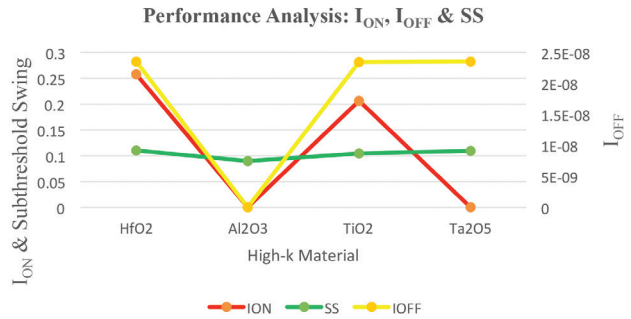

FIGURE 6. Results of I_{ON}, I_{OFF} and SS at different dielectric material

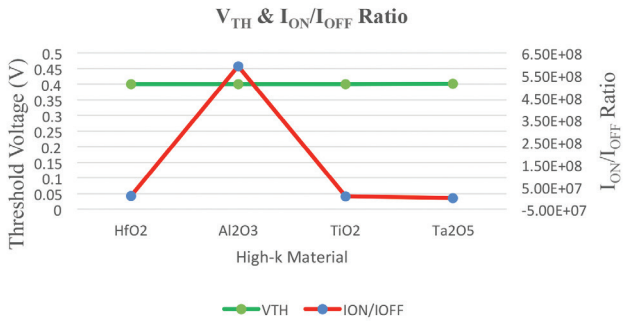

FIGURE 7. Results of I_{ON}/I_{OFF} at fixed V_{TH}

fixed V_{TH}. The results of this work which utilized the same graphene physical properties as the benchmarked device demonstrate a good performance which can be utilized for future design and optimization.

CONCLUSION

Fabrication process of the 60 nm gate length graphene field effect transistor was presented and significant physical features of graphene layer were characterized and measured based on the effective mass calculation and ballistic transport assumption. The performance of the device has been confirmed through the benchmarking with the established DESSIS model transistor of the same gate length which is fit for study and analysis of the design parameters. It must be conceded that the variations and profusion of Silicon S/D doping concentration in this research have formed a Schottky tunnelling junctions and lead to competitive I_{ON} and a very low $I_{OFF.}$ The performance evaluation between the gate oxides shows that the utilization of Al_2O_3 High-k material on graphene layers is capable in improving the switching capability of the device due to high I_{ON} to I_{OFF} ratio. The dependence of the device performance on the dielectric material can be observed.

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REFERENCES

Afifah Maheran, A.H., Menon, P.S., Ahmad, I. & Shaari, S. 2014. Effect of halo structure variations on the threshold voltage of a 22nm gate length NMOS transistor. *Materials Science in Semiconductor Processing* 17: 155-161.

Berger, C., Song, Z., Li, T., Li, X., Ogbazhi, A.Y., Feng, R., Dai, Z., Marchenkov, A.N., Conrad, E.H., First, P.N. & de Heer, W.A. 2004. Ultrathin epitaxial graphite: 2D electron gas properties and a route toward graphene-based nanoelectronics. *J. Phys. Chem B*. 108: 19912-19916.

Cheli, M., Fiori, G. & Iannaccone, G. 2009. A semi-analytical model of bilayer-graphene field effect transistor. *IEEE Transactions on Electron Devices* 56: 2979-2986.

Durkop, T., Getty, S.A., Cobas, E. & Fuhrer, M.S. 2004. Extraordinary mobility in semiconducting carbon nanotube. *Nano Letters* 4: 35-39.

Ferrari, A.C., Meyer, J.C., Scardaci, V., Casiraghi, C., Lazzeri, M., Mauri, F., Piscanec, S., Jiang, D., Novoselov, K.S., Roth, S. & Geim, A.K. 2006. Raman spectrum of graphene and graphene layers. *Physical Review Letters* 97: 187401. DOI: 10.1103/PhysRevLett.97.187401

Fiori, G., Bonaccorse, F., Iannaccone, G., Palacios, T., Neumaier, D., Seabaugh, A., Banerjee, S.K. & Colombo, L. 2014. Electronics based on two-dimensional materials. *Review Article Nature Nanotechnology* 9: 768-779. doi:10.1038/nnano.2014.207.

Kaharudin, K.E., Salehuddin, F., Zain, A.S.M. & Aziz, M.N.I.A 2016. Design and optimization of TiSix/HfO2 channel vertical double gate NMOS device. *IEEE Transactions on Electron Devices*. pp. 69-73.

Nemes-Incze, P., Osváth, Z., Kamarás, K. & Biro, L.P. 2008. Anomalies in thickness measurements of graphene and few layer graphite crystals by tapping mode atomic force microscopy. *Carbon* 46: 1435-1442.

Noor Faizah, Z.A., Ahmad, I., Ker, P.J. & Menon, P.S. 2016a. Process characterization of 32nm semi analytical bilayer graphene-based MOSFET. *MATEC Web Conf., IConGDM2016* 78: 1-6.

Noor Faizah, Z.A., Ahmad, I., Ker, P.J., Siti Munirah, Y., Mohd Firdaus, R., Mah, S.K. & Menon, P.S. 2016b. Statistical modelling of 14nm n-types MOSFET. *Journal of Telecommunication Electronic and Computer Engineering, JTEC* 8: 91-95.

Zhu, J. & Woo, J.C.S. 2007. Novel graphene channel field effect transistor with Schottky tunneling source and drain. *European Solid State Device Research Conference*. pp. 243-246.

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